

This cross-sectional view shows a substrate 24 with a base layer 20. Two active regions are formed on the substrate, each containing a stack of layers 26, 32, and 34. A gate stack 30 is positioned over each active region, with a gate dielectric layer 36 and a gate electrode layer 40. A channel layer 28 is located between the gate stack and the active region. A dashed line 10 indicates the top surface of the device.

FIGURE 2
PRIOR ART

10022297.121201

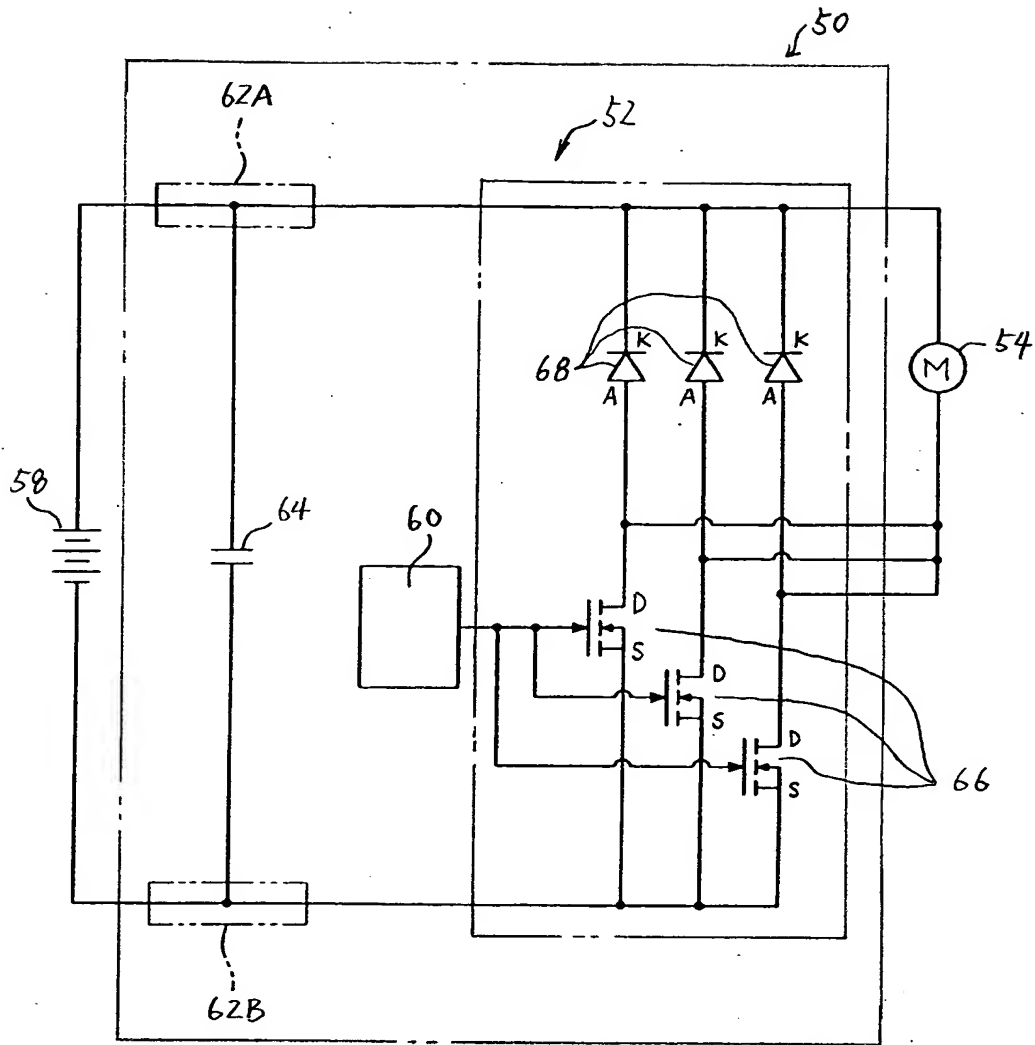
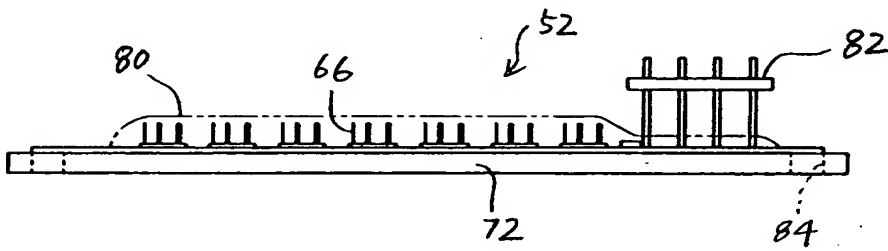
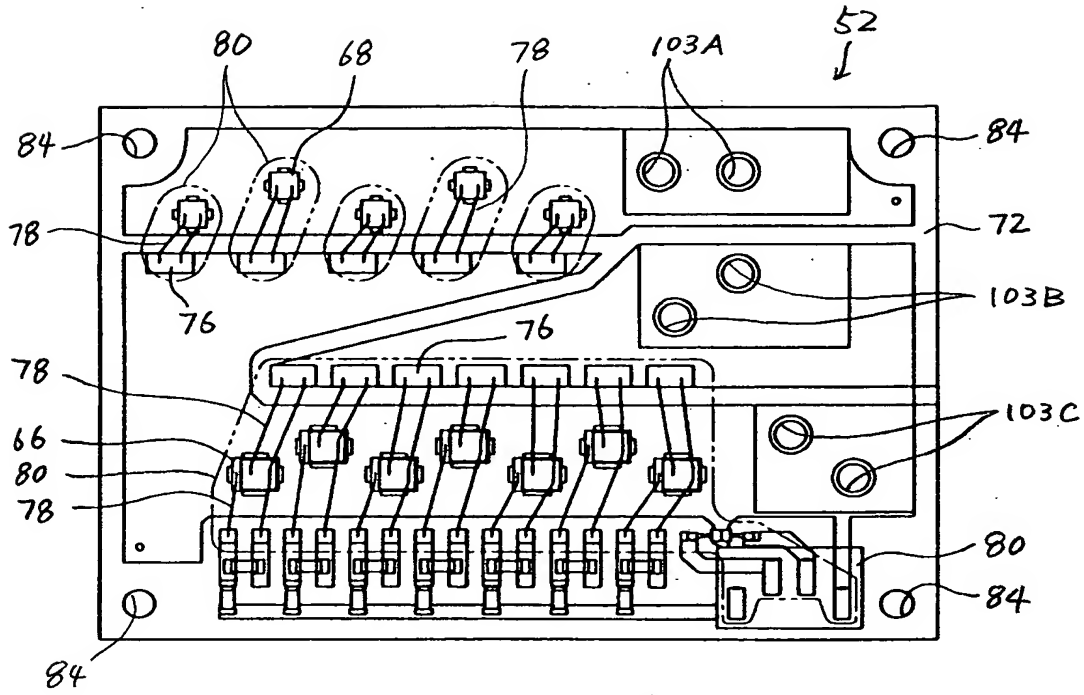


FIGURE 3

10022297 121201



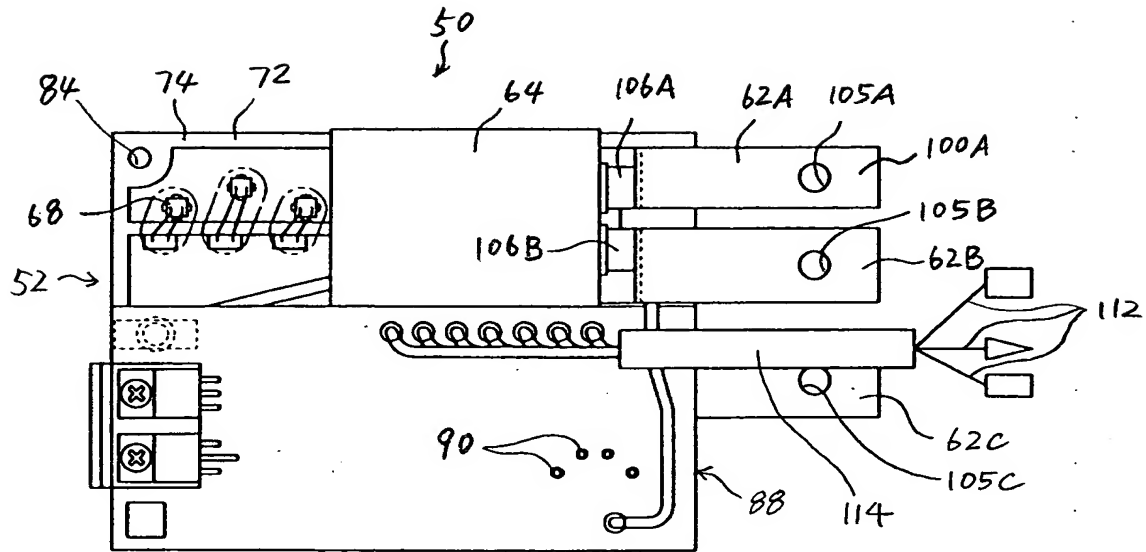


FIGURE 6

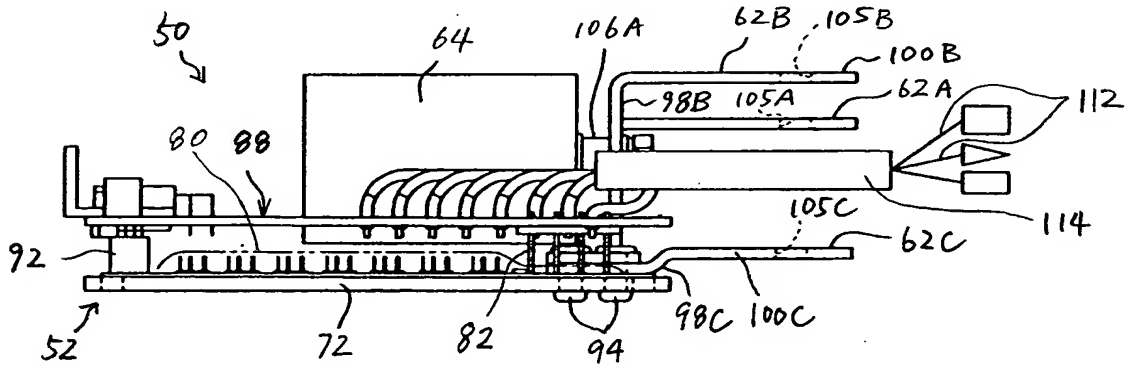


FIGURE 7

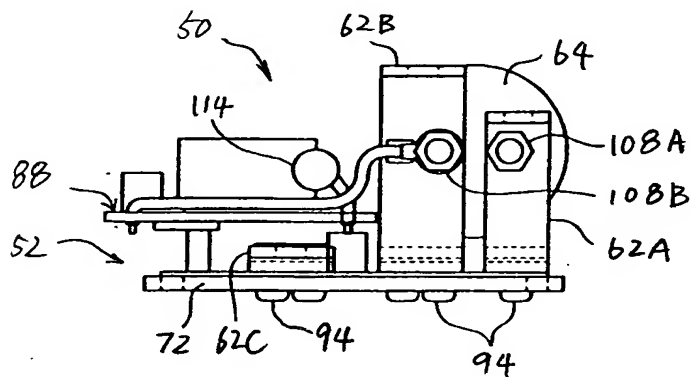


FIGURE 8

1002297 121201

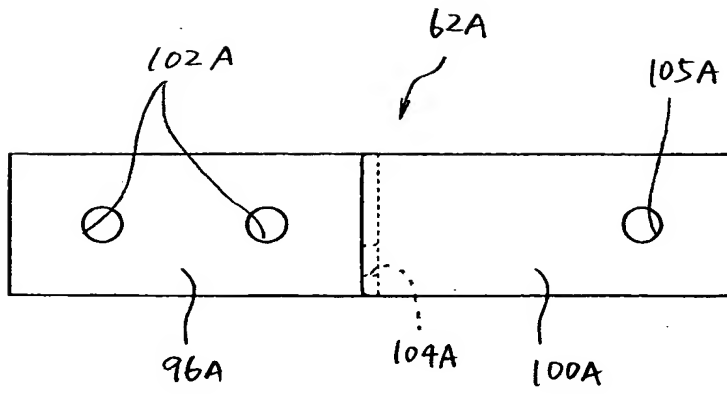


FIGURE 9

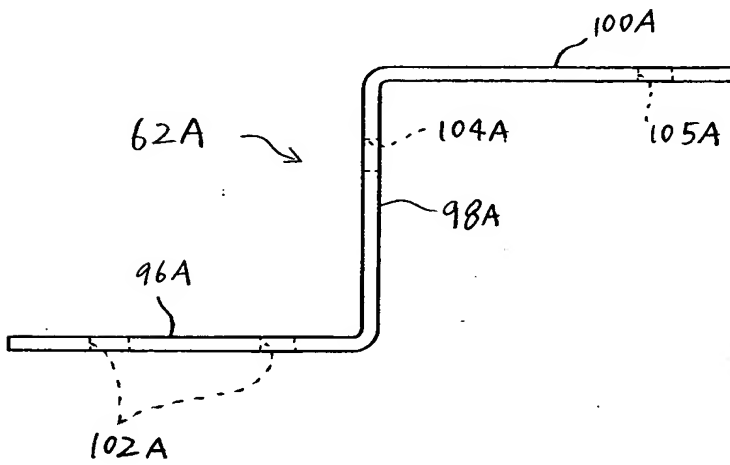


FIGURE 10

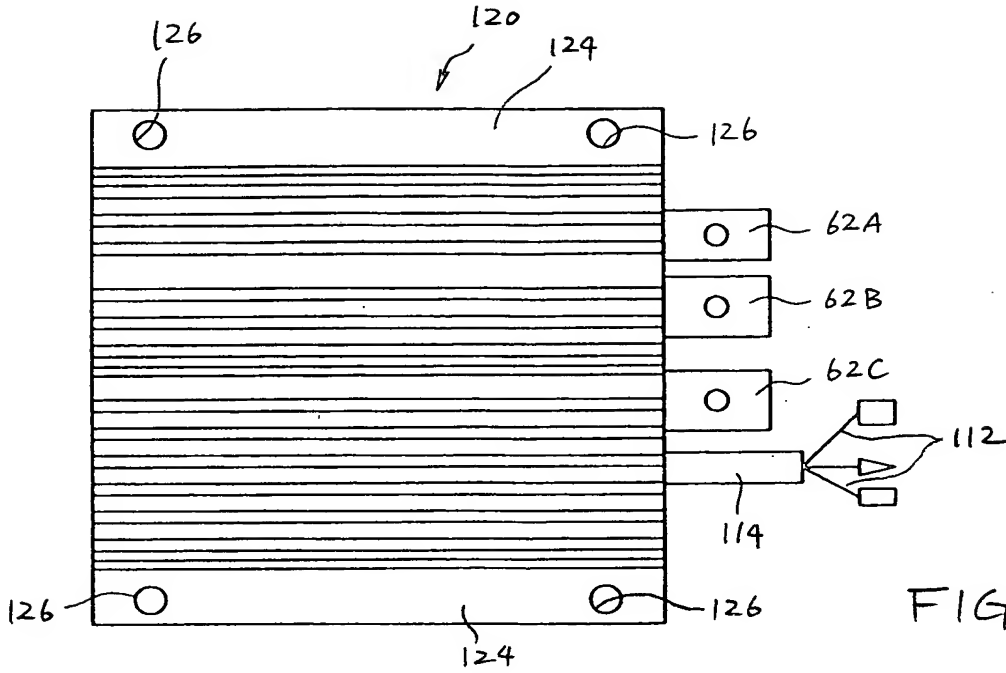


FIGURE 11

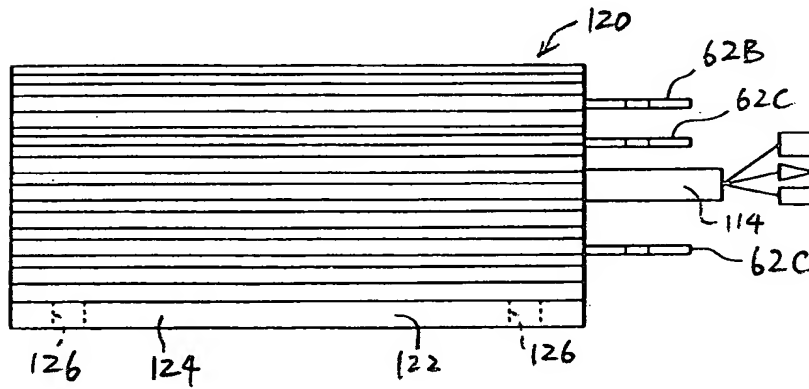


FIGURE 12

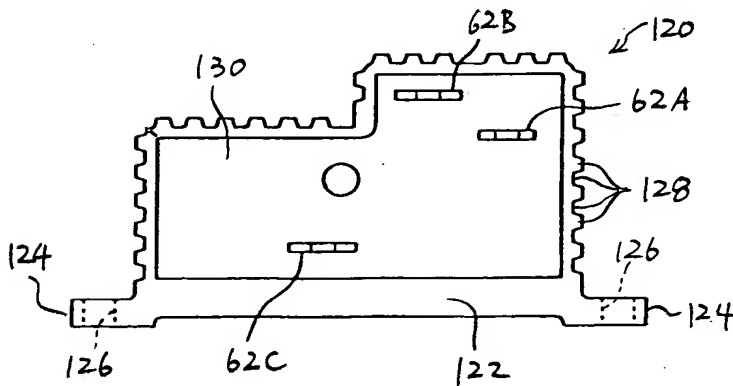


FIGURE 13

10022297.121201

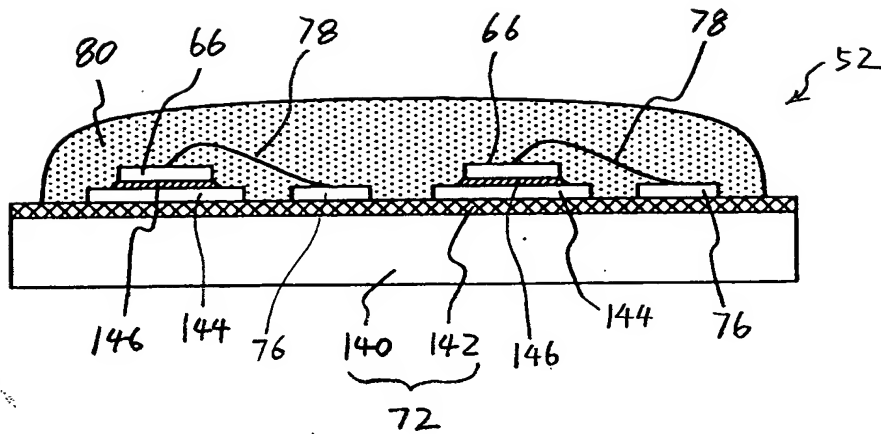


FIGURE 14

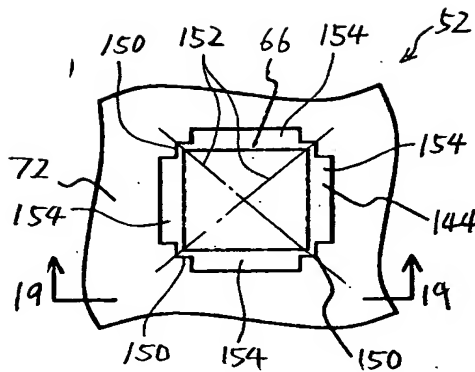


FIGURE 15

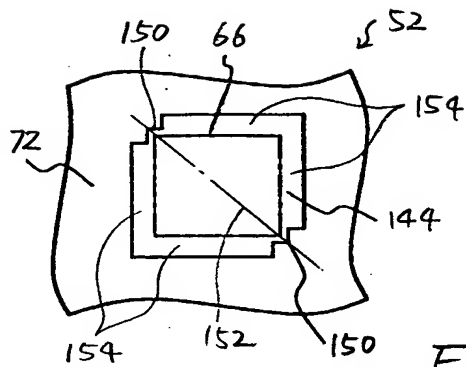


FIGURE 16

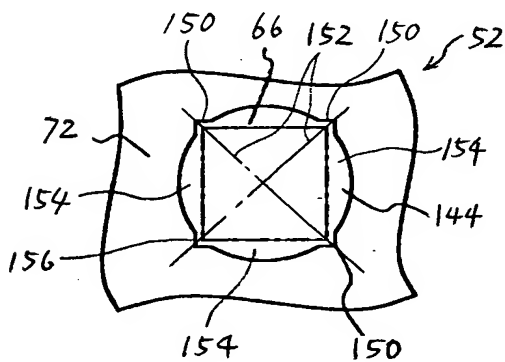


FIGURE 17

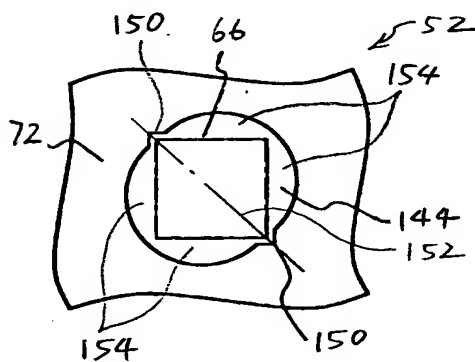


FIGURE 18

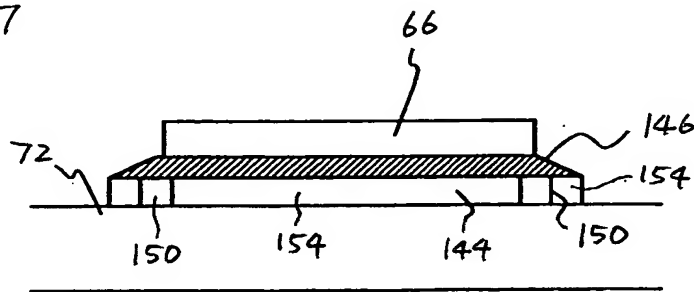


FIGURE 19

REFLOW SOLDERING DEVICE

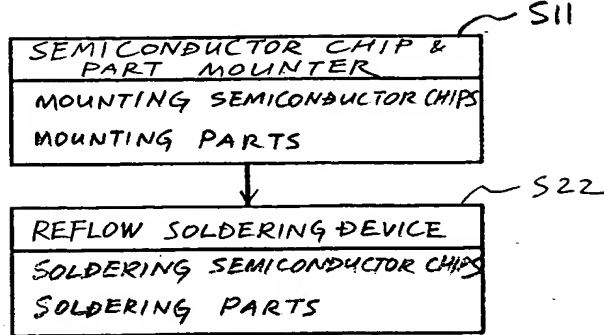


FIGURE 20

REFLOW SOLDERING DEVICE + DIE BONDER

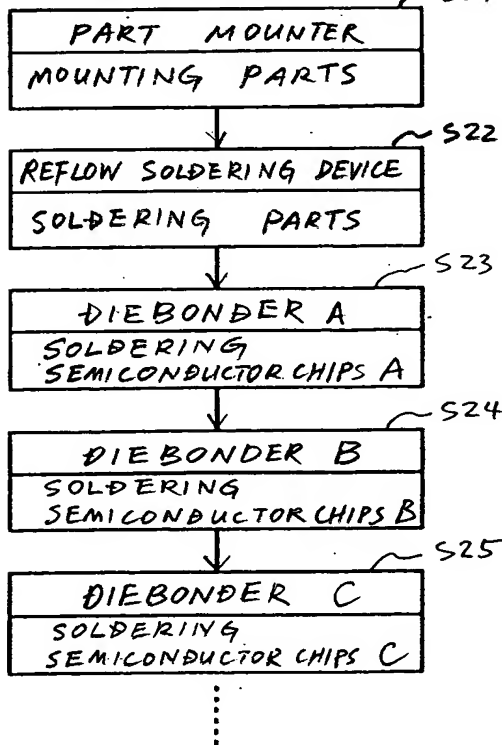


FIGURE 21

REFLOW SOLDERING DEVICE (USING MOUNTING JIG FOR SEMICONDUCTOR CHIPS)

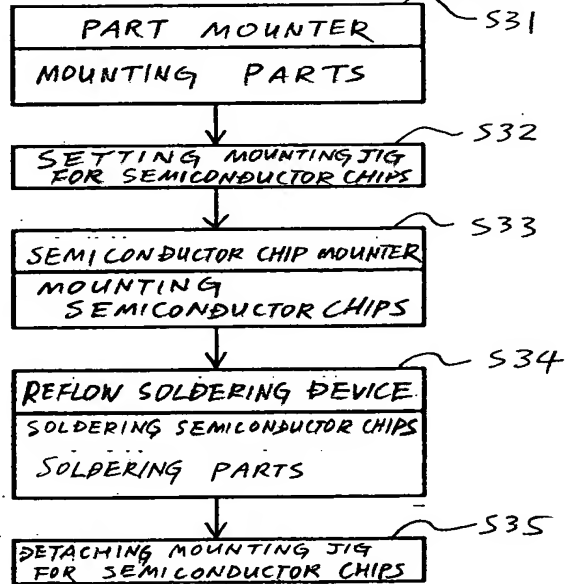


FIGURE 22

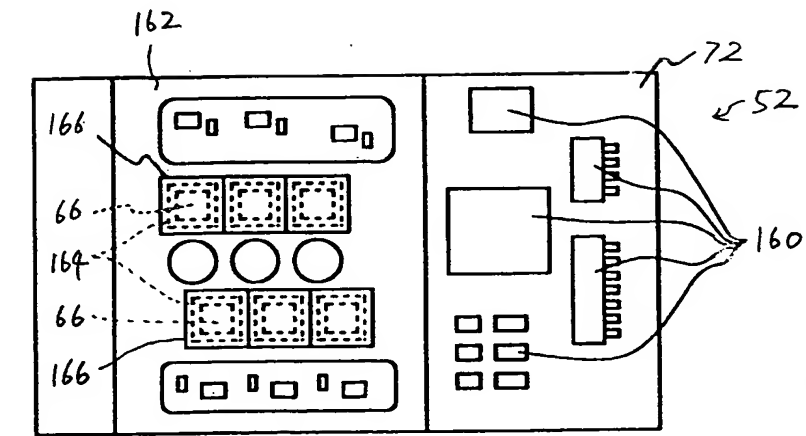


FIGURE 23

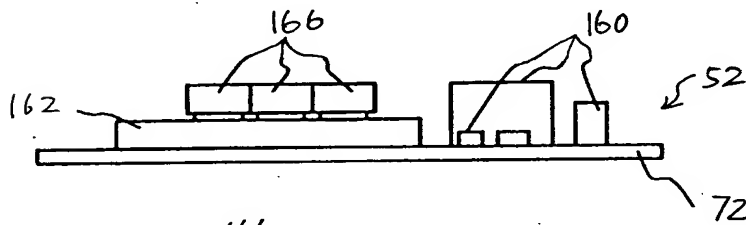


FIGURE 24

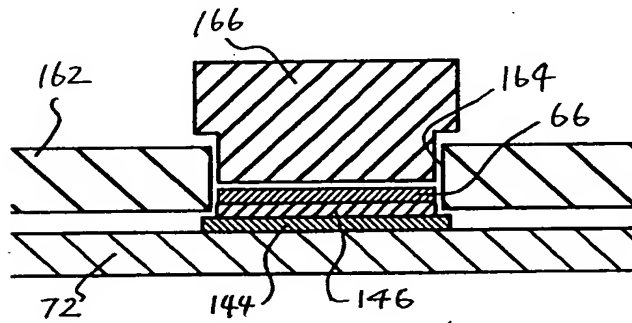


FIGURE 25

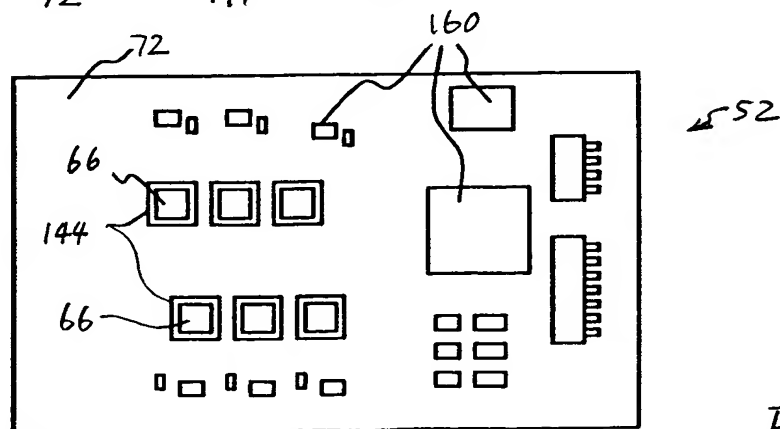


FIGURE 26